Image Manipulation IP core

The Image Manipulation IP core (in following text, we will use abbreviation IMIP) is an universal unit connected to AXI-lite and AXI-stream interface, that is designed to block-process (image) data. The core itself presents only a simplified interface that is capable to transfer data-block from/to system memory. The operation of the IMIP is implemented in set of modules, that are connected to internal bus of the unit. Modules shares some of configuration registers and user is allowed to select proper data-manipulating operation.

Schematics

IM IP core is composed of modules depicted in the figure:

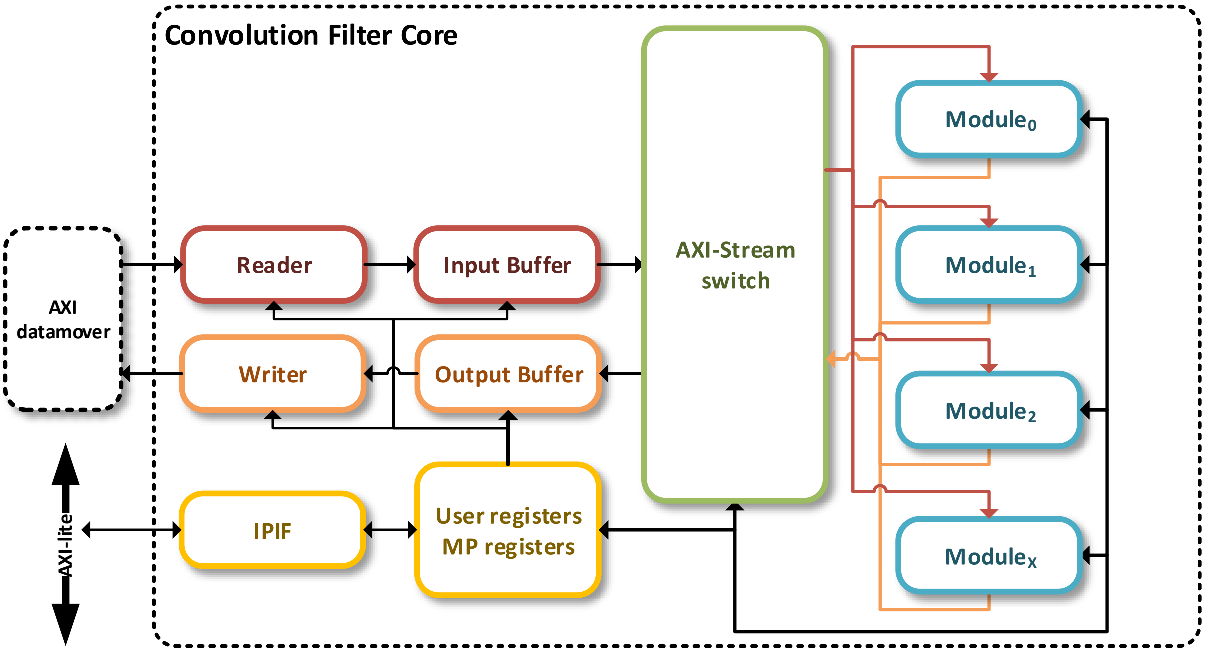

Figure 1: Block schematics of IMIP

The reader module reads data from user defined address in the system memory and streams them into Input Buffer FIFO (AXI-Stream FIFO 32 bit/2048 words). The output of the FIFO is connected to the AXI-Stream switch that switches reading form Input Buffer to computing modules. Outputs of computing modules are connected to the switch as well. The output data are buffered in the Output Buffer FIFO that has the same parameters as Input Buffer. IMIP is controlled via set of user registers accessible through the IPIF module connectable to the AXI-lite interface.

Beside the basic control set registers, there is also a small set of Multi-Purpose registers that are designed to control function of computing modules. There are 17 32-bit registers that are shared among all modules.

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User registers of IMIP

All registers are 32 bit, byte accessible. The address map is in the .

Register	Offset
Control and Status	0x00
Read Address	0x04
Write Address	0x08
Read Size	0x0C
Write Size	0x10
Interrupt	0x14
N/A	0x18 – 0x38
Multi-purpose 0 - 16	0x3C – 0x7C

Control register

Control register controls resets of IMIP submodules, data transfers and selection of operation type. The status of on-going operation is accessible through control register:

Bit	Name	RW	Default	Description
0	Reset	RW	0	IMIP reset. Resets all registers to their default states.
1	AXISRD reset	RW	0	Reader module & Input Buffer reset.
2	AXISWR reset	RW	0	Writer module & Output Buffer reset.
3	Module reset	RW	0	Module reset
4	Reserved	NA	0	NA
5	Run	RW	0	Runs the selected operation
6	Auto self-reset	RW	0	When set (1) auto-resets the module after operation.
[9:7]	Mode	RW	0	Sets the active computing module. Currently available are: Value: Mode 000: DMA 001: Convolution 010: Coloring 011: Gray
[23:16]	Reader last status	R	?	AXISRD status. 0x80 is successful operation. See [] for details.
[31:24]	Writer last status	R	?	AXISWR status. 0x80 is successful operation.

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Transfer registers

The set of transfer registers control transfer parameters. Read Address and Write Address registers holds addresses of source and destination memory pointers. Read Size and Write Size sets sizes of transfer in bytes. The sizes of read and write transfer might differ depending on the selected operation.

Bit	Register Name	RW	Default	Description
[31:0]	Read Address	RW	0	System address that will be read by the IMIP. It has to be accessible via selected AXI-Stream interface.
[31:0]	Write Address	RW	0	System address that will be written to by the IMIP. It has to be accessible via selected AXI-Stream interface.
[22:0]	Read size	RW	0	Size of read bytes. Maximum 8388604.
[22:0]	Write size	RW	0	Size of written bytes. Maximum 8388604.

Interrupt register

IMIP generates only single interrupt signal – transfer done that is activated by successful or erroneous transfer.

Bit	Name	RW	Default	Description
0	Global enable	RW	0	Global interrupt enable. When 0 disables generation of interrupt.
1	Transfer done enable	RW	0	Enables interrupt caused be finished transfer. Active in 1.
2	Transfer done status	RW	0?	Status bit of the transfer done interrupt.

Modules

Convolution Filter

Convolution filter module computes user parametrizable operation of 2D convolution over input data matrix (an image). The 5×5 convolution is defined as:

$$Pout_{i,j} = DivR \times \sum_{r=-2}^{r=2} \sum_{c=-2}^{c=2} Coef_{c,r} \times Pix_{i+c,j+r}$$

Where *$Pout_{i,j}$* is resulting pixel, *DivR* is reciprocal value of weighted sum division. *$Coef_{c,r}$* is a 5x5 matrix containing weights, and *$Pix_{i,j}$* is 5x5 neighboring of pixel. Indexes *c(olumn)* and *r(ow)* represents neighborhood of the pixel. The weighted sum and division is computed concurrently. Maximum length of the row is 1024 pixels (might be changed), number of rows is not limited. The module is controlled via Multi-purpose registers 0 - 16.

MP register of convolution filter module

The coefficients of weighted sum are stored in Fix16.8 numeric format (<-128,127.9961>), pixel values are supposed to be Fix16.0 (<-32768, 32767>), or less. The numeric format of reciprocal division

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depends on actual settings. It might be interpreted as Fix16.8 or Fix16.15(<-2,1.99994>). All register in the table are read/write accessible.

Name	MP index	Default	Description
Coef00	MP0 [15:0]	0	Coefficients CoefYX, where Y is the index of the row, and X is the index of the column. Each 32 bit register contains pair of coefficient values.
Coef01	MP0 [31:16]	0	
Coef02	MP1 [15:0]	0	
Coef03	MP1 [31:16]	0	
Coef04	MP2 [15:0]	0	
Coef10	MP2 [31:16]	0	
Coef12-Coef42	MP3-MP11	0	
Coef43	MP11 [31:16]	0	
Coef44	MP12 [15:0]	0	
DivR	MP12 [31:16]	0	Reciprocal division value.
DivR format	MP16 [0]	0	If set as 0, the DivR is interpreted as Fix16.8, otherwise as Fix16.15.

The operating conditions of the convolution operation are stored in four registers: Line Limit, Valid Limit, Valid Delay and Last Delay. Line Limit register sets the horizontal dimension of the image (width), Valid Limit controls delay between first incoming and the first out coming pixel. Delay register have to be set to their default value, hence their control internal parameters of the convolution core.

Name	MP index	Default	Description
Line limit	MP13 [11:0]	0	Sets the image width
Valid limit	MP14 [19:0]	0	Sets the delay between the first incoming and first processed pixel. For 5×5 matrix it should be: VL = 3×Line Limit + 3 For 3×3 convolution VL = 2×Line Limit + 2
Valid delay	MP15 [3:0]	0	These bits has to be set to 9.
Last delay	MP15 [7:4]	0	

Coloring module

The coloring module maps images from gray-scale (maximum range of UFix16) to the HOT pallet:

Coloring is stored in RGB24 color format.

Coloring module registers

The conversion is controlled using triplet of registers described in following table. There are two basic modes of operation – static and dynamic. In the static mode the range of the input data is supposed

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to be fixed between all frames. In the dynamic mode, the user is supposed to change range of input data for each frame.

Name	MP index	Default	Description
Minimum	MP0 [15:0]	0	Minimum defines the smallest value of input data.
Range	MP1 [15:0]	0	Range = Max – Min / 3. The format is UFix16.0. The maximum is the highest value of the input.
Div	MP2 [15:0]	0	Output normalization coefficient. It is supposed to be computed using formula: Div = 256*256 / Range. Div uses UFix16.8 numeric format.

Grayscale conversion module

The module converts high range gray-scale input format into 8bit gray scale output. It uses following equation:

$$Y_8 = \frac{(X_{16} - O_{16}) \times G_{16.10}}{1024}$$

X is the input data in UFix16.0 numeric format, O is offset with the same format, G is Gain (Fix16.10). The output Y uses Fix8.0 format. Four adjacent pixels are stored in single 32bit output word.

Name	MP index	Default	Description
Byte Swap	MP0 [0]	0	Output data endianness. 0 – little, 1 big endian.
Offset	MP1 [15:0]	0	Minimum of input data.
Gain	MP2 [15:0]	0	Gain.

Coming soon

Hence the architecture is modular, it is easy to add more functions to the IMIP. The following modules will be available soon:

Colorspace conversion, Gearbox-switch module, Gamma Correction module.

IMIP parameters

Although it is parametrizable, at the given time it is not recommended to change some of the generic parameters of the IMIP.

Jméno	Výchozí	Význam
C_S_AXIS_MM2S_TDATA_WIDTH	32	Reader AXI-Stream data width.
C_S_AXI_MM2S_ADDR_WIDTH	32	Reader AXI-Stream address width.
C_M_AXIS_S2MM_ADDR_WIDTH	32	Writer AXI-Stream data width.
C_M_AXIS_S2MM_TDATA_WIDTH	32	Writer AXI-Stream address width.
C_COEF_WIDTH	16	Convolution coefficient width.

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C_FIFO_WIDTH	36	Convolution FIFO width.
C_MAX_LINE_WIDTH	11	Base 2 Log of the maximum image width.
C_MAX_PIXEL_NUM	20	Base 2 Log of the maximum image size.
C_KERNEL_SIZE	5	Maximum convolution kernel size.

Resource utilization and characteristics were obtained using Xilinx ISE 14.7 and Zynq7020 -1 device.

Resource	Usage
LUT	2206
Register	2558
DSP48E1	28
BRAM 36K	7
Maximum frequency	212,9 MHz

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